Notice of References Cited	Application/Control No. 10/673,501	Applicant(s)/Patent Under Reexamination MITROVIC, ANDREJ S.	
	Examiner Akash Saxena	Art Unit 2128	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,802,045	10-2004	Sonderman et al.	703/22
	B	US-6,615,097	09-2003	Ozaki, Hiroji	703/22
	C	US-5,719,796	02-1998	Chen, Vincent Ming Chun	703/13
	D	US-6,905,895	06-2005	Coss et al.	438/16
	E	US-6,812,045	11-2004	Nikoonahad et al.	438/14
	F	US-6,774,998	08-2004	Wright et al.	356/401
	G	US-6,763,277	07-2004	Allen et al.	700/100
	H	US-6,757,645	06-2004	Chang et al.	703/13
	I	US-6,728,591	04-2004	Hussey et al.	700/121
	J	US-6,643,616	11-2003	Granik et al.	703/13
	K	US-6,628,809	09-2003	Rowe et al.	382/115
	L	US-6,618,856	09-2003	Coburn et al.	717/135
	M	US-6,571,371	05-2003	Coss et al.	716/4

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Emerging Paradigms in Semiconductor Manufacturing"; Paul P. Castrucci; 1990 Int'l Semiconductor Mfg. Science Symposium; IEEE 1990
	V	"Mathematic-Physical Engine: Parallel Processing for Modeling and Simulation of Physical Phenomena"; V.K.Jain et al; IEEE 1994
	W	"Conceptual Framework for Manufacturing Service Provisioning by Virtual Fabs"; Yea-Huey Su et al; 1998 NSC Republic Of China; 1998 Semiconductor Mfg. Technology Workshop.
	X	"New approaches for Simulation of Wafer Fabrication: The Use of Control Variates and Calibration Metrics" Chanettre Rasmidatta et al; Proceedings of 2002 Winter Simulation Conference; 2002

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/673,501	Applicant(s)/Patent Under Reexamination MITROVIC, ANDREJ S.	
	Examiner Akash Saxena	Art Unit 2128	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,866,437	02-1999	Chen et al.	438/14
	B	US-2003/0078738	04-2003	Wouters et al.	702/22
	C	US-2004/0044513	03-2004	Kitahara, Noriaki	703/017
	D	US-2004/0078319	04-2004	Madhavan et al.	705/038
	E	US-2004/0102934	05-2004	Chang, Fang-Cheng	703/001
	F	US-2005/0016947	01-2005	Fatke et al.	216/002
	G	US-2005/0010319	01-2005	Patel et al.	700/121
	H	US-2004/0078319	04-2004	Madhavan et al.	705/038
	I	US-2003/0135302	07-2003	Hung et al.	700/245
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Detailed Simulation for Semiconductor Manufacturing"; Robert W. Atherton et al; Proceedings of the 1990 Winter Simulation Conference
	V	"Integrated CAM and Process Simulation to Enhance On-Line Analysis and Control of IC Fabrication"; Angus J. MacDonald et a; IEE Transcations on Semicinductor Mfg. Vol.3 No.2 May 1990.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.